REMARKS

As a preliminary matter, Applicants note that the Examiner initialed the original Form PTO-1449 filed on December 11, 2001, and not the Substitute Form PTO-1449 filed on January 14, 2002. The Substitute Form PTO-1449 corrected an error related to the date of JP08115060A by correctly indicating the date as 5-7-96 (and not as 7-5-96 as on the original Form PTO-1449). Applicants respectfully request that the Examiner correct the record accordingly, and indicate that the record has been corrected in the next Communication with Applicants.

Claims 1-5 and 9-11 stand rejected under 35 U.S.C. § 103 as being unpatentable over United States Patent No. 6,144,355 to Murata et al. in view of United States Patent No. 4,713,691 to Tanaka et al. Applicants respectfully traverse this rejection.

Applicants respectfully submit that there is no motivation to combine the art of Tanaka et al. with the art of Murata et al. because the technical fields of each reference are different. Murata et al. relates to display on an LCD panel, and Tanaka et al. relates to printing out a video signal. Further, while the art of Murata et al. is directed to a control circuit to provide various signals to driver circuits to drive the LCD panel, the art of Tanaka et al. is directed to a video signal hard copy apparatus. Furthermore, while the art of Murata et al. is directed to controlling phases of signals to be provided to the driver circuits, the art of Tanaka et al. is directed to controlling delay of sampling clocks with respective to an input video sync signal.

Additionally, even if a person skilled in the art tries to combine the art of Tanaka et al. with the art of Murata et al., since data sampled by a data sampling circuit 3 and stored in an image memory 4 is used to determine a delay amount in a delay circuit 7 according to Tanaka et al. (see FIG. 1), the person should use data displayed on the LCD panel to control the phase delay amount, clearly unlike the configuration of the present invention.

In fact, according to the present invention, a delay amount of a clock signal or a data signal provided to a driving circuit 19 for driving a liquid crystal display panel 21 is controlled according to a time-series change of the data signal.

Accordingly, Applicants respectfully submit that one of ordinary skill in the art would not have been motivated to combine Murata et al. with Tanaka et al. to arrive at the claimed invention. Thus, Applicants respectfully request the withdrawal of this §103 rejection of Claims 1-5 and 9-11.

For all of the above reasons, Applicants request reconsideration and allowance of the claimed invention. Should the Examiner be of the opinion that a telephone conference

would aid in the prosecution of the application, or that outstanding issues exist, the Examiner is invited to contact the undersigned.

Respectfully submitted,

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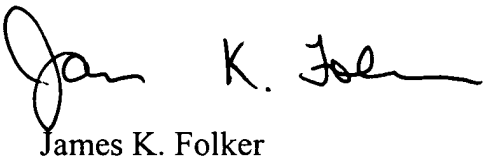
By 

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